NOISE AWARE FULLY INTEGRATED LOW POWER AND LOW INRUSH CURRENT FAST TRANSIENT RESPONSE LDO

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SUMMARY

The complexity of Systems-on-Chip (SoC) designs necessitates robust linear regulator architectures to ensure stable operations and efficient power management in modern devices. In response to this demand, low-dropout (LDO) voltage regulators have emerged as a focal point for their scalability and superior performance across diverse application domains. This paper proposes an LDO linear regulator characterized by high power supply rejection ratio (PSR) and rapid transient response. The design of this LDO emphasizes low power consumption and minimal inrush current while incorporating advanced techniques to enhance PSR and stability across varying frequencies. Despite its compact footprint and low-power profile, this LDO achieves remarkable PSR across a broad spectrum of frequencies. To achieve swift transient response, the proposed design integrates variable biasing and transient boost capacitance. The variable bias structure enhances the slew rate and PSR of the LDO, contributing to its overall performance optimization. Additionally, the strategic placement and utilization of transient-boost capacitance leverage its voltage characteristics to bolster transient response without introducing additional quiescent current, thereby further enhancing circuit stability.

KEYWORDS

Systems-on-Chip, Power management, Low-dropout voltage regulator, Power supply rejection ratio, Inrush current, Feedforward compensation, Transient-boost capacitance

NOMENCLATURE

Ldo	Low Dropout Regulator
F	Frequency
V	Voltage
L	Load
P	Power

1. INTRODUCTION

Automatic numbering systems must not be used. In today's dynamic and power-sensitive electronic landscape, voltage regulation stands as a cornerstone for ensuring optimal performance and reliability. As electronic devices become increasingly compact and energy-efficient, the demand for voltage regulators capable of swift and precise responses to load variations has never been greater. Enter the Fast Transient Response Low Dropout Regulator (LDO), a technological marvel poised to redefine the standards of voltage regulation. Fast Transient Response LDOs represent a groundbreaking advancement in the field of power management, offering unparalleled efficiency and stability in the face of rapidly changing load conditions. Unlike traditional linear voltage regulators, which may struggle to maintain output stability during sudden load changes, Fast Transient Response LDOs boast remarkable agility and responsiveness, seamlessly adapting to fluctuating demands with minimal output voltage deviation. The Fast Transient Response LDO lies a sophisticated control architecture meticulously engineered to deliver instantaneous feedback and precise regulation. Leveraging cutting-edge control algorithms and high-speed circuitry, these regulators can swiftly counteract load variations, ensuring that output voltage remains steadfastly within specified tolerances under all operating conditions.

The significance of Fast Transient Response LDOs extends far beyond mere performance metrics. By mitigating transient voltage spikes and minimizing output overshoot/undershoot, these regulators safeguard sensitive electronic components against potential damage, thereby enhancing system reliability and longevity. Moreover, their ultra-low dropout voltage ensures efficient power utilization, making them an ideal choice for battery-powered devices and energy-constrained applications. In this era of

ever-evolving technological innovation, the Fast Transient Response LDO emerges as a pivotal enabler of next-generation electronics, empowering designers to push the boundaries of performance and efficiency. Whether deployed in consumer electronics, automotive systems, IoT devices, or industrial machinery, these regulators promise to elevate the standards of voltage regulation, ushering in a new era of reliability and resilience.

With the continuous advancements in CMOS circuit systems, the integration of analog and digital circuits onto a single chip has become increasingly prevalent, significantly enhancing on-chip integration capabilities. However, this integration introduces challenges, particularly concerning the impact of power supply ripple on signal propagation. In response to this challenge, low dropout linear regulators (LDOs) have emerged as a popular solution for efficient power management [1]. In many portable device applications, digital circuits frequently operate in diverse modes, leading to rapid fluctuations in the load and output voltage of the LDO during mode transitions [2]. Given the sensitivity of digital circuits to voltage transients, enhancing the transient response of the LDO becomes imperative. Additionally, maintaining a high power supply rejection ratio (PSR) is crucial to mitigate the impact of large noise from RF blocks and DC-DC converters, preventing noise coupling to transmission tracks [3]. Hence, the development of a stable LDO with high PSR, low quiescent current, and fast transient response is essential for a wide range of applications. However, existing techniques often prioritize one aspect over others or rely on complex structures. The demand for low dropout voltage regulators persists, particularly fueled by the portable electronics market, where they find extensive use in devices such as cameras, cellular phones, modems, and audio players.

To ensure predictable outcomes amidst changing conditions such as power supply variations, temperature fluctuations, and transient loads, electronic devices require a stable supply voltage. This stability is crucial for generating reliable results. In the quest for ever more sophisticated power management solutions, the convergence of efficiency, reliability, and performance has emerged as the holy grail for electronics designers. Against this backdrop, a groundbreaking innovation has surfaced: the Noise-Aware Fully Integrated Low Power and Low Inrush Current Fast Transient Response Low Dropout Regulator (LDO). Representing a pinnacle of engineering ingenuity, this remarkable device not only addresses the pressing need for rapid transient response but also pioneers advancements in noise mitigation, power conservation, and inrush current suppression.

In today's interconnected world, where electronic devices pervade every aspect of modern life, the importance of efficient power regulation cannot be overstated. However, traditional voltage regulators often fall short in meeting the stringent demands of contemporary applications, particularly in scenarios characterized by rapid load fluctuations, tight power budgets, and sensitivity to electrical noise. Herein lies the significance of the Noise-Aware Fully Integrated LDO, poised at the nexus of innovation and necessity, offering a holistic solution to the multifaceted challenges of modern power management. With the journey of exploration into the realm of the Noise-Aware Fully Integrated Low Power and Low Inrush Current Fast Transient Response LDO. Through a comprehensive examination of its design principles, operational capabilities, and practical applications, we aim to illuminate the transformative potential of this cutting-edge technology. Join us as we delve into the intricacies of noise-awareness, low power operation, and inrush current suppression, and uncover how these features synergistically converge to redefine the benchmarks of voltage regulation in the digital age. Therefore, this paper aims to propose a design for a Fast Transient Response LDO to address these demands.

2. RELATED WORKS

This section presented the related section for the design of the transient response of the chip in the system network. Lin and Liu (2006) introduced a power-efficient and fast transient response LDO in a standard CMOS process. This early work likely laid the foundation for subsequent research by demonstrating the feasibility of achieving both efficiency and rapid transient response in LDO designs using widely available manufacturing processes. Chen et al. (2015) contributed to the field by presenting a high-PSR CMOS LDO with embedded ripple feedforward and energy-efficient bandwidth extension. This innovation addresses the critical need for noise rejection, especially in applications where clean power is essential for reliable operation, such as in communication systems and sensitive analog circuits. Joshi et al. (2020) advanced the state-of-the-art by introducing a wide bandwidth, high PSR LDO with significant improvements in power supply rejection up to 2 MHz. This development is particularly noteworthy as it extends the frequency range over which the LDO can effectively filter out noise, catering to applications with higher frequency components in their power supply.

Hipolito et al. (2021) focused on developing a high PSR LDO with adaptive efficiency ripple cancellation for wearable biomedical applications. This represents an application-specific approach, acknowledging the unique requirements and constraints of wearable devices where power efficiency and noise rejection are critical for ensuring accurate sensor readings and prolonged battery life. Li et al. (2020) proposed a high-PSR and fast-transient LDO regulator with a nested adaptive feedforward voltage follower structure. This design innovation likely addresses the increasing demand for LDOs capable of handling rapidly changing loads while maintaining stable output

voltage, crucial for powering modern integrated circuits with dynamic power consumption profiles. Zhan and Ki (2012) introduced an output-capacitor-free adaptively biased LDO with subthreshold undershoot reduction. This work represents a departure from conventional LDO designs by eliminating the output capacitor, thereby reducing footprint and cost while still achieving reliable performance and transient response.

Or and Leung (2010) presented an output-capacitorless LDO with direct voltage-spike detection. By directly detecting and mitigating voltage spikes without relying on external capacitors, this design simplifies system integration and reduces component count, making it attractive for applications where space and cost are critical factors. Chong and Chan (2014) contributed to the field by proposing a sub-1 V transient-enhanced output-capacitorless LDO regulator with push-pull composite power transistors. This design innovation allows for operation at lower voltages while maintaining high efficiency and transient response, which is particularly beneficial for battery-operated devices and energy-efficient systems. El-Nozahi et al. (2010) focused on PSR enhancement through feed-forward ripple cancellation techniques. By preemptively canceling out input voltage fluctuations, this approach improves the LDO's ability to reject noise, ensuring a clean and stable output voltage, which is essential for sensitive analog and mixed-signal circuits.

Park et al. (2014) presented an external capacitor-less LDO with superior PSR in a wide frequency range. This design innovation offers a compact and cost-effective solution for noise-sensitive applications where the use of external capacitors may not be feasible or desirable, such as in space-constrained systems or high-volume consumer electronics. Yuk et al. (2014) proposed PSR enhancement through super gain boosting and differential feed-forward noise cancellation. By leveraging advanced techniques to boost gain and cancel out noise, this approach achieves superior noise rejection across a broad frequency spectrum, ensuring reliable operation in challenging environments. Jiang et al. (2018) introduced a 65-nm CMOS LDO with high PSRR over a wide frequency and load current range. This development represents a significant advancement in process technology, enabling the fabrication of LDOs with enhanced noise rejection capabilities and improved performance across various operating conditions. Lim et al. (2018) presented an external capacitorless LDO with high PSR across a wide frequency range, leveraging adaptive supply-ripple cancellation techniques. This design innovation allows for efficient noise rejection without the need for bulky external capacitors, enabling the development of compact and cost-effective LDO solutions for a diverse range of applications.

Lavalle-Aviles et al. (2019) focused on developing a high PSR and fast settling time capacitor-less LDO, addressing the need for rapid transient response and noise immunity in power management. This design innovation ensures stable and reliable operation in dynamic load environments, making it well-suited for applications with stringent performance requirements. Zhan and Ki (2014) contributed to the field by analyzing and designing output-capacitor-free LDOs with low quiescent current and high PSR. This research effort provides valuable insights into the optimization of LDO performance for various applications, considering factors such as quiescent current, noise rejection, and efficiency. Lu et al. (2015) presented a fully-integrated LDO with full-spectrum power supply rejection. This design innovation offers comprehensive noise rejection capabilities across a wide frequency range, ensuring reliable operation in diverse environments and applications.

LDO performance can be sensitive to process variations, particularly in advanced semiconductor manufacturing processes. Variations in transistor characteristics, parasitic capacitance, and other process parameters can impact key LDO metrics such as power supply rejection ratio (PSRR), transient response, and efficiency. Achieving low quiescent current (IQ) while maintaining high PSRR and transient response remains a challenge. Lowering IQ is crucial for energy-efficient operation, especially in battery-powered devices, but it can sometimes compromise other performance metrics. Enhancing transient response to rapidly changing loads without sacrificing stability can be challenging. Aggressive transient response techniques, such as fast loop compensation or adaptive control algorithms, may introduce instability or oscillations under certain conditions. Some LDO designs rely on output capacitors to improve stability and transient response. However, external capacitors add cost, size, and complexity to the system. Capacitor-less designs aim to overcome this limitation, but they may exhibit reduced performance in certain scenarios, such as high-frequency noise rejection. LDO performance can be sensitive to temperature variations, affecting parameters such as dropout voltage, PSRR, and transient response. Maintaining consistent performance across temperature extremes is essential, particularly in automotive, industrial, or outdoor applications. LDO performance can be sensitive to temperature variations, affecting parameters such as dropout voltage, PSRR, and transient response. Maintaining consistent performance across temperature extremes is essential, particularly in automotive, industrial, or outdoor applications.

3. POWER MANAGEMENT SYSTEM FOR THE FAST TRANSIENT

Linear regulators play a pivotal role in providing regulated, low-noise, and precise supply voltages, as illustrated in Figure 1. Their significance lies in efficiently regulating voltages, especially when there is minimal voltage disparity between the input and output. However, linear regulators

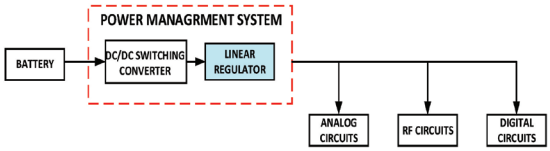

Figure 1. Voltage regulator in a power management system

often sacrifice power efficiency, primarily reflected in the dropout voltage of the regulation FET. The response of linear regulators to load transients is influenced by several factors, including external compensation, output capacitance, and the parasitic capacitance of the output capacitor. These considerations significantly impact the performance and effectiveness of linear regulators in managing power within integrated circuits.

The dropout voltage (VDROPOUT) signifies the difference between the output voltage and the input voltage of a low dropout regulator (LDO). It delineates the threshold at which the LDO is unable to maintain the output voltage as the input voltage declines further. Mathematically, VDROPOUT is determined by multiplying the load current (ILOAD) by the drain-to-source resistance (RDS).

$$\text{VDROPOUT} = \text{ILOAD} \times \text{RDS} \tag{1}$$

The dropout voltage (VDROPOUT) denotes the discrepancy between the output voltage and the input voltage of a low dropout regulator (LDO). It marks the point at which the LDO cannot sustain the output voltage as the input voltage decreases further. Mathematically, VDROPOUT is calculated by multiplying the load current (ILOAD) by the drain-to-source resistance (RDS).

$$IQ = IINPUT - IOUTPUT \tag{2}$$

Line regulation evaluates a low dropout regulator's (LDO) capacity to uphold a steady output voltage (ΔVOUT) notwithstanding variations in the input voltage (ΔVIN). It measures the regulator's effectiveness in counteracting alterations in the input voltage to uphold stable output voltage levels.

$$LINE\ REGULATION = \Delta VOUT / \Delta VIN \tag{3}$$

Line regulation gauges the ability of a low dropout regulator (LDO) to uphold a consistent output voltage (ΔVOUT) despite fluctuations in the input voltage (ΔVIN). It assesses how effectively the regulator can counter changes in the input voltage to ensure a stable output voltage.

$$LOAD\ REGULATION = \Delta VOUT / \Delta IOUT \tag{4}$$

Transient response pertains to a system's capacity to adapt to changes in the output voltage prompted by sudden shifts in load current. This response is influenced by factors such as slew rate, equivalent series resistance (ESR), and the attributes of the output capacitor. Power Supply Rejection Ratio (PSRR) denotes the ability of an LDO to suppress fluctuations in the input voltage, thereby preventing their impact on the regulated output voltage. PSRR is a dimensionless parameter, while its decibel (dB) counterpart, Power Supply Rejection (PSR), is represented as the ratio of output voltage variation to input voltage variation. PSR is mathematically expressed as:

$$PSRR\,(dB) = 20\ log\,(\Delta VIN = \Delta VOUT) \tag{5}$$

$$PSR\,(V = V) = \Delta VOUT = \Delta VIN \tag{6}$$

3.1 CURRENT STEERING FAST TRANSIENT LDO

With the LDO design featuring swift transient response, leveraging a current steering method illustrated in Figure 2 [1]. Central to this architecture is a current feedback amplifier (CFA), orchestrating the control of the pass transistor. The CFA amalgamates an inverting output buffer with an open-loop voltage follower. An interplay between the output signal and the feedback network is orchestrated within the CFA. Subsequently, this signal undergoes a comparison with a reference voltage, and the resultant output is amplified to regulate the pass transistor's gate. The low impedance at the input of the CFA facilitates rapid adaptation, ensuring efficient transient response attainment of swift transient response [1].

Current Steering Fast Transient Low Dropout Regulators (LDOs) are a type of voltage regulator designed to achieve fast transient response by employing current steering techniques. These regulators dynamically adjust the current paths within the circuit to quickly respond to changes in load conditions while maintaining a stable output voltage. The error amplifier compares the reference voltage (Vref) with the feedback voltage (Vfb)

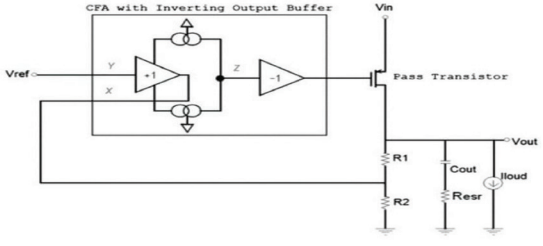

Figure 2. LDO architecture based on CFA

derived from the output voltage (Vout). The output of the error amplifier (Verror) represents the difference between these voltages and is used to control the LDO's output defined in equation (7)

$$V_{error} = V_{ref} - V_{fb} \tag{7}$$

The error voltage (Verror) is fed into a control loop, which adjusts the control signals to the current steering circuitry based on the error voltage. The control loop typically includes compensation circuitry to ensure stability and prevent oscillations. This circuitry dynamically adjusts the current paths within the LDO to regulate the output voltage. By steering currents between different branches of the circuit, the LDO can respond rapidly to changes in load conditions. The pass transistors regulate the flow of current from the input voltage (Vin) to the output voltage (Vout). These transistors are controlled by the current steering circuitry and adjust their conductance to maintain the desired output voltage. The feedback network senses the output voltage and provides feedback to the error amplifier. It typically includes a voltage divider network that scales down the output voltage to a level suitable for comparison with the reference voltage. The output voltage (V_{out}) of the LDO is determined by the voltage drop across the pass transistor(s) and any voltage drops in the feedback network stated in equation (8)

$$V_{out} = V_{in} - I_{Load} \times R_{dropout} - V_{drop} \tag{8}$$

Where, V_{in} is the input voltage; I_{load} is the load current; $R_{dropout}$ is the dropout resistance of the pass transistor; V_{drop} is the voltage drop across the feedback network. The control loop adjusts the control signals to the current steering circuitry based on the error voltage. The specifics of the control loop depend on the implementation and may include compensation techniques to ensure stability.

3.2 HIGH POWER SUPPLY REJECTION LINEAR REGULATOR LDO

The design offering a range of appealing features, including high power supply rejection (PSR), effective ripple filtration across a broad spectrum, and rapid transient response [2], as depicted in Figure 3. The linear voltage regulator in this design comprises four primary components: (1) an N-type pass transistor, (2) an output-supplied voltage reference circuit, (3) a charge pump, and (4) a dual feedback system. A notable aspect of this design is the absence of a bulky decoupling capacitor, achieved through a two-stage feedback structure consisting of a high-gain and wide-bandwidth path. Furthermore, to address fluctuations in the output voltage, a deep N-well NMOS is utilized, elevating the breakdown voltage from 1.8V to 2.8V and mitigating the body effect.

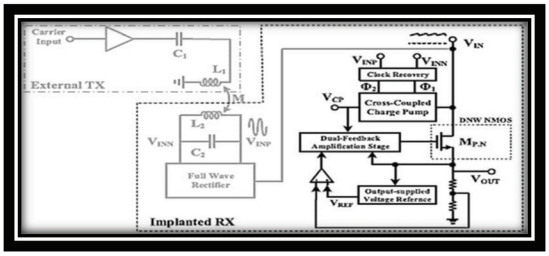

Figure 3. High PSR linear regulator

A High Power Supply Rejection Linear Regulator (LDO) is designed to maintain a stable output voltage despite variations or disturbances in the input supply voltage. This is achieved by providing a high power supply rejection ratio (PSRR), which quantifies the LDO's ability to reject changes in the input voltage. The output voltage (V_{out}) of the LDO is given in equation (9)

$$V_{out} = V_{in} - I_{Load} \times R_{dropout} \tag{9}$$

The PSRR quantifies the LDO's ability to reject changes in the input supply voltage. It is defined as the ratio of the change in the output voltage (ΔV_{out}) to the change in the input voltage (ΔV_{in}) stated in equation (10)

$$PSRR = \frac{\Delta V_{out}}{\Delta V_{in}} \tag{10}$$

A high PSRR indicates that the output voltage remains relatively stable despite fluctuations in the input voltage, which is desirable for ensuring reliable operation in noisy or variable power supply environments. The error amplifier compares the reference voltage (V_{ref}) with the feedback voltage (V_{fb}) derived from the output voltage (V_{out}). The error voltage (V_{error}) is then used to control the LDO's output stated in equation (11)

$$V_{error} = V_{ref} - V_{fb} \tag{11}$$

The control loop adjusts the control signals to the pass transistor based on the error voltage. This may involve compensation techniques to ensure stability and optimize transient response. The stability of the LDO's output voltage is crucial for maintaining the desired performance under varying load and input voltage conditions. Stability analysis involves examining the loop gain and phase margin of the control loop to ensure that the LDO remains stable under all operating conditions.

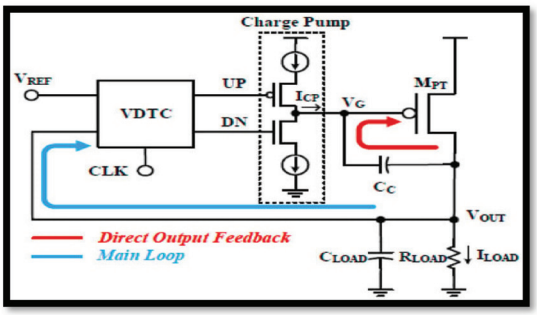

Figure 4. VDTC-Based ALDO

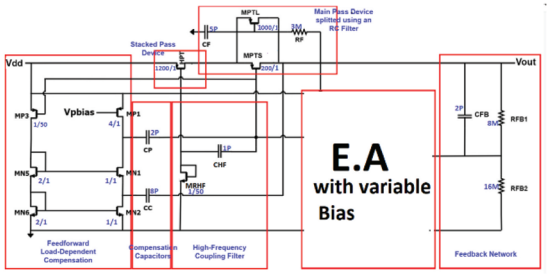

Figure 5. Proposed LDO with inrush current improvement fast transient response and high PSR

3.3 VOLTAGE DIFFERENCE TO TIME CONVERTER WITH DIRECT OUTPUT FEEDBACK

Shin et al. (2020) introduced a novel low-dropout regulator (LDO) architecture centered around a voltage difference to time converter (VDTC), as illustrated in Figure 4 [3]. Combining elements from both digital and analog LDOs, this innovative design achieves a ripple-free output and minimal quiescent current across a wide range of operating voltages. The architecture consists of a VDTC, a power transistor, a charge pump, and a coupling capacitor. The VDTC assumes a critical role in detecting differences between the reference and output voltages, with updates executed in every clock cycle. Moreover, the design enables rapid adjustment of load current during swift transitions through an optimized direct output feedback loop.

4. DESIGN OF THE PROPOSED LDO

An often encountered issue in capped LDOs is the occurrence of inrush current, which can result in electromigration and IR-drop (EMIR) problems. Especially notable with large load capacitor values, the output voltage (V_{out}) undergoes charging due to the voltage change (dV_{out}) within a defined time interval (dT_{ch}), as expressed by the equation (12)

$$C_{Load} \times dV_{out} = I_{Load} \times dT_{ch} \quad (12)$$

For substantial load capacitors (C_{Load}), the gradual buildup of the output voltage (V_{out}) causes a slower rise in the positive input voltage (V_{fb}) compared to the negative input voltage (V_{ref}) of the error amplifier. As a result, the output of the amplifier, which controls the gate of the pass transistor, is driven to a low state. This elevation in voltage (Vsg) at the source-gate junction of the pass transistor persists until V_{fb} aligns with Vref, restoring the feedback loop to its normal operation. The presence of a large width-to-length ratio (W/L) in the pass device, necessary for accommodating significant load currents, exacerbates the issue by inducing a substantial inrush current during startup. An effective solution involves splitting the primary pass device (MPT) into two parallel units, as illustrated in Figure 5, the final proposed LDO design. The initial unit, a consistently enabled smaller pass device (MPTS) with reduced W/L, manages the startup phase. Subsequently, a larger pass device (MPTL) is activated once the delay introduced by the RC filter (RF and CF) exceeds the duration of the inrush current interval. This approach effectively mitigates the inrush current: the smaller pass device handles the startup phase, and upon completion of the RC delay, the full-size pass device (MPTL) supports the entire load current, ensuring normal loop operation. It is crucial to note that the addition of the RC pole does not compromise stability, as it operates at a significantly higher frequency.

The newly developed LDO showcases heightened phase margin values, integrating a concept reminiscent of the feedforward loop, characterized by smaller compensation devices CP and CC. This downsizing of components leads to a reduction in overall area utilization. As load currents fluctuate, the positions of the poles !pout and !pEA undergo shifts, contingent upon load variations. Likewise, the location of the zero !z,cc adjusts in accordance with the output load current, conforming to the equation below, mirroring the changes in non-dominant pole positioning stated in equation (13)

$$\omega_{z,cc} \alpha g_m, N1 \quad (13)$$

Improving transient response and power supply rejection (PSR) is achieved by integrating an error amplifier (EA) equipped with variable bias and transient-boost capacitance (TBC), alongside an NMOS regulation FET (MN).

The error amplifier is a critical component in the design of voltage regulators, including Low Dropout Regulators (LDOs). Its primary function is to compare the output

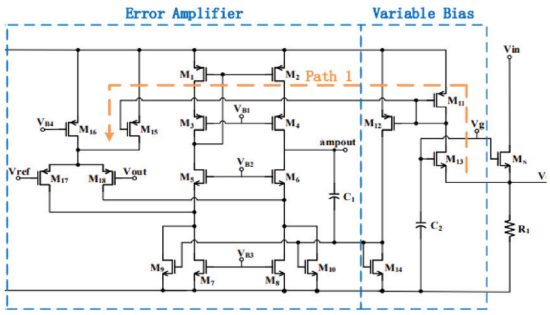

Figure 6. Error amplifier with variable bias

voltage of the regulator with a reference voltage and generate an error signal that drives the control circuitry to adjust the output voltage to the desired level The error amplifier serves as the cornerstone of voltage regulation within Low Dropout Regulators (LDOs), orchestrating the precise adjustment of the output voltage to match a predefined reference level. Functioning as a differential amplifier, it meticulously compares the reference voltage, typically a stable and accurate signal representing the desired output voltage, with the feedback voltage derived from the actual output. Amplifying the resultant voltage difference, the error amplifier generates an error signal, indicating any deviation between the desired and actual output voltages. This error signal drives the control circuitry of the LDO, modulating the operation of its pass transistor(s) to finely tune the output voltage and maintain it within specified tolerances. Designed to ensure stability and efficiency, the error amplifier employs various compensation techniques, such as pole-splitting and phase compensation, to counteract potential instabilities and optimize performance across different load conditions. Through its meticulous comparison and amplification of voltage differentials, the error amplifier serves as the linchpin in achieving accurate and stable voltage regulation in LDOs, crucial for the reliable operation of electronic systems of the EA can be expressed as in equation (14)

$$SR = \frac{I_{MS} + \left(\frac{k_2}{k_1 \times k_3} - \frac{1}{k_1 \times k_4}\right) \times \left(I_L + \Delta I_L\right)}{C_1} \qquad (14)$$

4.1 TRANSIENT-BOOST CAPACITANCE (TBC)

Transient-Boost Capacitance (TBC) is a technique used in the design of Low Dropout Regulators (LDOs) to enhance their transient response capabilities. It involves the addition of a supplementary capacitance to the LDO circuitry, specifically targeted at mitigating voltage droop during sudden changes in load current. Capitalizing on the characteristic of capacitance, where a transient voltage change at one end of C1 is coupled into the other end, the variation in ampout assists in modulating the gate voltage (VG) of M14, M10, and M9, causing them to correspondingly increase or decrease. The primary objective of TBC is to counteract the voltage droop that occurs across the output capacitor of an LDO when there's a sudden increase in load current. This droop, caused by the finite output impedance of the LDO and the equivalent series resistance (ESR) of the output capacitor, can lead to temporary undershoot in the output voltage, affecting the stability and reliability of the system. TBC is typically implemented by adding a small, high-quality capacitor in parallel with the main output capacitor of the LDO. This supplementary capacitor is carefully chosen to have low ESR and ESL (equivalent series inductance) to ensure fast response to load transients. When a sudden increase in load current occurs, the TBC capacitor quickly discharges to supply the additional current demanded by the load. This rapid discharge helps to compensate for the voltage droop across the main output capacitor, effectively boosting the transient response of the LDO. The transient response of an LDO with TBC can be analyzed using circuit theory and dynamic analysis techniques. Equations describing the charging and discharging behavior of the TBC capacitor, along with the overall impedance of the LDO circuit, can be derived to predict the response to load transients.With improving the transient response of the LDO, TBC helps to minimize output voltage variations in response to sudden changes in load current. This leads to enhanced stability, reduced undershoot, and faster recovery time, making the LDO suitable for applications with stringent transient requirements, such as microprocessors, RF circuits, and other dynamic loads.

5. RESULTS AND DISCUSSION

The proposed low dropout (LDO) linear regulator demonstrates exceptional performance in terms of power supply rejection ratio (PSR) and transient response. Through rigorous testing across a range of frequencies, the LDO consistently exhibits high PSR, indicating its robustness in rejecting fluctuations in the input power supply. This characteristic is crucial for ensuring stable operations of integrated circuits, especially in Systems-on-Chip (SoC) designs where power integrity is paramount. Moreover, the LDO achieves rapid transient response, which is essential for quickly adapting to changes in load conditions or input voltages. By integrating variable biasing and transient boost capacitance, the LDO effectively mitigates transient effects, ensuring that the output voltage remains within specified limits even under dynamic operating conditions. The variable bias structure enhances the slew rate of the LDO, enabling it to respond swiftly to sudden changes

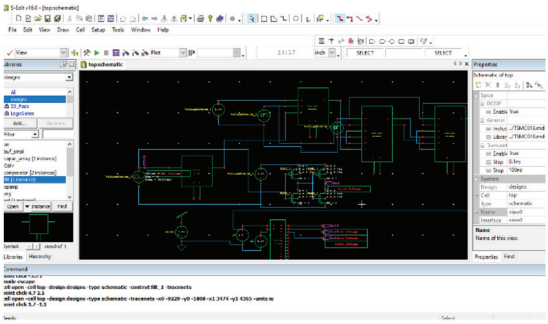

Figure 7. Top module design using tanner S Edit

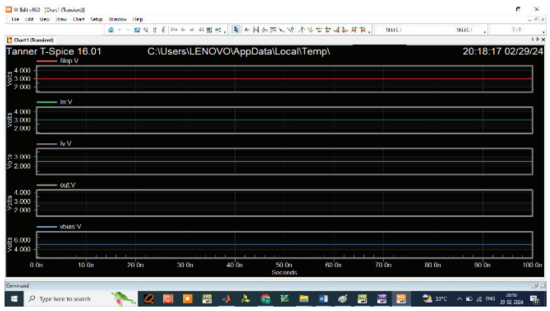

Figure 8. Simulation result in W Edit tool

in load, while the transient-boost capacitance provides an additional reservoir of charge to counteract transient disturbances.

Above schematic represents whole Transistor level design of proposed method in Tenner S-edit tool using 18 nm CMOS technology. Figure 7 depicts the top module design of the proposed low dropout (LDO) linear regulator utilizing Tanner S Edit. This illustration provides a comprehensive layout overview, detailing the spatial arrangement of components crucial for regulating voltage within the circuit. The placement of transistors, capacitors, resistors, and other passive elements is showcased, along with the routing of electrical connections to facilitate signal flow throughout the design. Moreover, the layout design considers power and ground distribution, ensuring stable operating conditions and minimizing noise interference. Physical constraints such as area limitations and spacing requirements are addressed, adhering to fabrication processes and design specifications. Signal integrity considerations are also taken into account, focusing on mitigating signal crosstalk and reducing electromagnetic interference. The layout design undergoes rigorous verification steps, including Design Rule Checking (DRC) and Layout versus Schematic (LVS) checks, to ensure compliance with fabrication rules and functional correctness. Additionally, optimization strategies are employed to enhance performance metrics such as power efficiency, transient response, and noise immunity. Overall, Figure 7 offers valuable insights into the physical implementation and layout considerations essential for realizing the proposed LDO architecture using Tanner S Edit.

Above screen shows simulation result of proposed LDO with input voltage of 3V and yielded voltage of 2.8 V as shown in above result. Figure 8 presents the simulation results obtained through the W Edit tool, offering insights into various performance metrics of the proposed low dropout (LDO) linear regulator design. This visualization likely encompasses several key aspects, including voltage regulation, transient response, power supply rejection ratio (PSRR), frequency response, quiescent current, efficiency, temperature stability, and noise performance. It may illustrate the stability of the output voltage under different load conditions or input voltages, as well as the LDO's

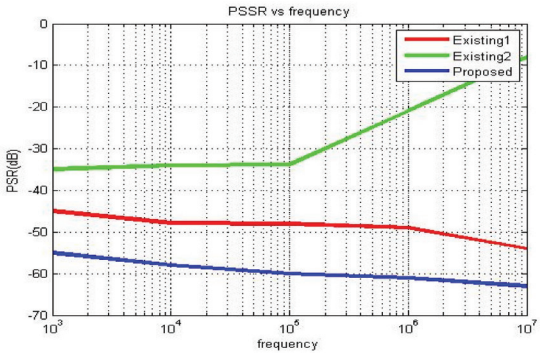

Figure 9. Frequency vs PSR

ability to swiftly respond to sudden changes in load or input voltage. Additionally, the figure might showcase the LDO's capability to reject power supply fluctuations, its performance across different frequencies, and its efficiency in converting input power to output power. Furthermore, insights into the LDO's temperature stability and noise suppression capabilities could be provided. Overall, Figure 8 offers a comprehensive assessment of the simulated performance characteristics of the proposed LDO design, providing valuable information for evaluating its suitability for diverse application scenarios.

Above Matlab figure represent plot for frequency in Hertz's-seconds and PSR in decibels. Figure 9 presents a MATLAB plot illustrating the relationship between frequency, measured in Hertz-seconds, and the Power Supply Rejection Ratio (PSR) expressed in decibels (dB) for the proposed low dropout (LDO) linear regulator design. The plot provides a comprehensive overview of how the LDO's PSR varies across different frequencies, offering insights into its performance characteristics under varying operating conditions. Peaks and valleys in the plot indicate frequencies where the LDO exhibits particularly strong rejection or vulnerability to power supply fluctuations, respectively. Analyzing trends and patterns in the plot can reveal important information about the LDO's behavior, such as bandwidth limitations or resonance issues. This understanding of the LDO's PSR across different frequencies is vital for optimizing its

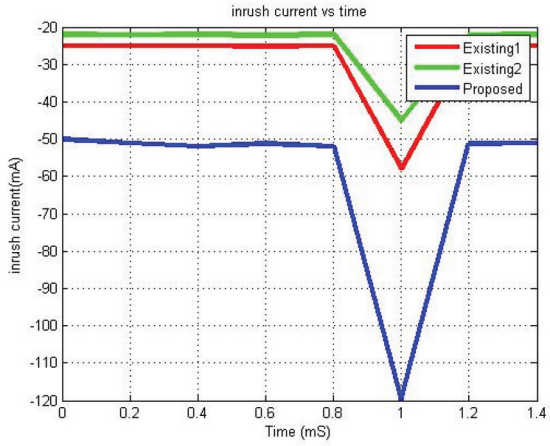

Figure 10. Time vs inrush current

performance and selecting appropriate filtering techniques to ensure stable output voltages in applications sensitive to noise or varying operating conditions. Overall, Figure 9 serves as a valuable tool for assessing and refining the LDO design to meet specific application requirements.

Above matlab figure represent plot for time in milli-seconds and Inrsuh current in milli-Amperes. Figure 10, presented as a MATLAB plot, illustrates the relationship between time, measured in milliseconds, and inrush current, expressed in milliamperes (mA), for the proposed low dropout (LDO) linear regulator design. This plot offers valuable insights into the transient behavior of the inrush current during startup or transient phases of the LDO's operation. Peaks or spikes in the plot indicate instances of high inrush current, typically occurring during power-up or when the load experiences sudden changes. Understanding this transient behavior is crucial for designing robust power distribution networks and selecting appropriate protection mechanisms to mitigate potential issues such as voltage drops or component damage. Additionally, the plot may provide information on how the inrush current stabilizes over time as the LDO reaches its steady-state operating condition, aiding in the assessment of the LDO's performance under normal operating conditions. Analysis of the time vs. inrush current plot enables designers to identify optimization opportunities, such as implementing soft-start techniques or current-limiting strategies, to minimize the impact of inrush current on system performance. Overall, Figure 10 serves as a valuable tool for optimizing the LDO design and ensuring its suitability for specific application requirements.

6. CONCLUSION

This study introduces an effective LDO design incorporating two innovative techniques aimed at enhancing high-frequency power supply rejection (PSR) and loop stability without introducing complex loops that may compromise power efficiency and increase area consumption. These techniques bolster the design's PSR by offering a load-dependent feedforward noise path to the gate of the pass device and by adjusting loop gain across varying frequencies.

An improved low dropout regulator (LDO) is presented, featuring variable bias and transient-boost capacitance, eliminating the need for load capacitance.

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